UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,298	12/31/2003	Kyung-Hoon Kim	51876P560	9780

8791 7590 02/24/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,298	KIM, KYUNG-HOON	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: On page 13, lines 16-18, the sentence beginning "Also, if a clock period of the low frequency," appears to be grammatically incorrect. The sentence appears to be lacking some additional information.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Inaba et al. (U.S. Patent No. 4,218,705).

In reference to claim 1, Inaba discloses in Figure 3 a delay line unit (80) comprising: a first delay line (82) having a plurality of first unit delays (while the figures do not show each unit delay, Inaba discloses in column 4, line 58 that the delay line may include taps indicating multiple delay units in a single delay line), each first unit delay having a first delay (the total equaling 8.33 milliseconds see column 4, lines 10-20); a second delay line (84) having a plurality of second unit delays (while the figures do not show each unit delay, Inaba discloses in column 4, line 58 that the delay line may include taps indicating multiple delay units in a single delay line), each second unit

delay having a second delay (the total equaling 16.7 milliseconds see column 4, lines 10-20); a third delay line (86) having a plurality of third unit delays (while the figures do not show each unit delay, Inaba discloses in column 4, line 58 that the delay line may include taps indicating multiple delay units in a single delay line), each third unit delay having a third delay (the total equaling 33.3 milliseconds see column 4, lines 10-20), wherein the first delay is shorter than the second delay, and the second delay is shorter than the third delay.

In reference to claim 2, Inaba discloses in Figure 3 that the first (82), second (84), and third (86) delays are connected in series.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 3 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (U.S. Patent No. 6,628,155).

In reference to claim 3, Park discloses in Figure 3 a delay locked loop (DLL) circuit used in a synchronous memory device, comprising: a phase comparing unit (110) for comparing a reference signal (ext) with a feedback signal (int) and generating a comparison signal; a delay controlling unit (104, 106) for generating a control signal in response to the comparison signal; a delay line unit (204, 302) for delaying an internal clock signal in response to the control signal; and a delay model (114, 112) for generating a feedback signal by delaying a clock signal, wherein the delay line unit (204, 302) includes a plurality of delay lines (204, 302) each delay line containing a

plurality of unit delays having a different unit delay, respectively. The same applies to claim 6.

5. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (U.S. Patent No. 6,836,166).

In reference to claim 1, Lin discloses in Figure 2 a delay line unit (208, 204) comprising: a first delay line (208) having a plurality of first unit delays, each first unit delay having a first delay (NxTCD); a second delay line (218) having a plurality of second unit delays, each second unit delay having a second delay (FD2); a third delay line (220) having a plurality of third unit delays (), each third unit delay having a third delay (CD2), wherein the first delay is shorter than the second delay, and the second delay is shorter than the third delay. The same applies to claims 4-5.

In reference to claim 2, Lin discloses in Figure 2 that the first (208), second (218), and third (220) delays are connected in series.

In reference to claim 3, Lin discloses in Figure 2 a delay locked loop (DLL) circuit used in a synchronous memory device, comprising: a phase comparing unit (228) for comparing a reference signal (CLKBUF) with a feedback signal (CLKFB) and generating a comparison signal; a delay controlling unit (212, 214) for generating a control signal in response to the comparison signal; a delay line unit (208, 218, 220) for delaying an internal clock signal in response to the control signal; and a delay model (226) for generating a feedback signal by delaying a clock signal, wherein the delay line unit (208, 218, 220) includes a plurality of delay lines each delay line containing a

plurality of unit delays having a different unit delay, respectively. The same applies to claim 6.

Allowable Subject Matter

6. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: Claims 7-8 would be allowable because the closest prior art of record fails to disclose a method wherein the step c) includes the steps of: c1) delaying the clock signal through a first delay line containing a plurality of first unit delays, each having a first resolution; c2), if a delay locking operation is not achieve in the step c1), delaying the clock signal through a second delay line containing a plurality of second unit delays, each having a second resolution, which is higher than the first resolution; and c3), if a delay locking operation is not achieved in the step c2), delaying the clock signal through a third delay line containing a plurality of third unit delays, each having a third resolution, which is higher than the second resolution in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-

1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

February 16, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800